The Care, Feeding, and Application of Unity Gain Buffers

Application Note | March 23, 1998 | AN1102

Unity gain buffers have been available in integrated form since the introduction of the LH0002 by National Semiconductor several years ago. The “ideal” buffer would exhibit a gain identically equal to one, an input impedance of infinity, an output impedance of 0Ω, infinite bandwidth and zero phase shift, infinite slew rate, large but limited to a safe level output current, and an output offset voltage and input bias current of zero. These devices are usually implemented with fairly simple circuit topologies which makes them very cost effective in applications requiring large output currents, isolation from reactive loads, input to output isolation, and in some instances thermal isolation in circuits requiring precision gain and offset. The buffers simplicity imply obvious applications in a circuit. After all, what could go wrong with a unity gain buffer? This note is intended to discuss this very subject.

Circuit Topologies

When you get down to it, there are only two types of circuits: open and closed loop. The latter are specially designed operational amplifiers optimized for operation at unity gain which typically exhibit less bandwidth, more phase shift, and usually more expensive than the open loop variety. On the other hand, they exhibit better offset voltage and gain linearity. The former is essentially a glorified compound emitter follower offering cost, increased bandwidth, and in general poorer DC characteristics.

Open Loop Buffers

Shown in Figure 1 is the classic “0002” topology. It is comprised of compound emitter followers Q1 and Q3 which provide current gain for positive going signals and their mirror image of Q2 and Q4 for negative signals. Bias is set up with current sources I1 and I2. In some realizations of the circuit, I1 and I2 are replaced by resistors. If we assume for simplicity that I1 = I2, inspection of the circuit reveals that the Vbe's of Q1 and Q2 are impressed across the base emitter junctions of Q3 and Q4; hence, the emitter currents of Q3 and Q4 are almost equal to I1 or I2 (ignoring the effects of R1 and R2). In real circuits, R1 and R2 are used to prevent thermal runaway of the output stage. Since Q3 and Q4 will sink or source many milliamps, their Vbe's will decrease as they heat up, but the “bias” voltage across them, $Vbe_{(Q1)}$ + $Vbe_{(Q2)}$ remains substantially the same, there is a real possibility of reaching a thermal runaway point. R1 and R2 provide “positive” feedback to the output transistors increasing their effective Vbe as the output current increases.

One of the nice things about the 0002 topology is that it exhibits very low crossover distortion (typically under 0.1% with an output power of 0.5W @ 10MHz). As the output current in Q3 increases, its Vbe increases while Q4's emitter current and Vbe decrease while the bias of $Vbe_{(Q1)}$ + $Vbe_{(Q2)}$ remains essentially constant. Q4's emitter current never quite goes to zero thus minimizing crossover distortion.

The output current will limit or the output voltage will “clip” when all the current provided by I1 (or I2) is demanded as base current to Q3 (or Q4) which obviously occurs when: $I1 = I_{OUT}/ß$ or when I1 saturates. The output offset voltage is simply the difference between Vbe_{Q1} and Vbe_{Q3} or Vbe_{Q2} and Vbe_{Q4} whichever is lower. To the first order then:

$$V_{OS} = Vbe_{Q1} – Vbe_{Q3} \text{ or } Vbe_{Q2} – Vbe_{Q4} \quad (1)$$

$$Ibias = I1\ (ß1 - ß2)/(ß1)(ß2) \quad (2)$$

$$A_V \cong R_L/(R_L + R_{OUT}) \quad (3)$$

$$R_{OUT} \cong [R1 + re_{Q4} + Rs/(ß4*ß1)]/2 \quad (4)$$

$$R_{IN} \cong (ß1)(ß2)(R_L) \quad (5)$$

$$I_{SUPPLY} \cong 3\ I1$$

Myth Number 1: Input Impedance

Earlier we said that one of the attributes of an ideal buffer was infinite input impedance. Illustrated in Figure 2 is a plot of the input impedance of the EL2002, 180MHz Unity Gain Buffer. Clearly, at low frequencies, the input impedance is above 1MΩ; however, as the frequency increases the ß decreases and the input impedance drops accordingly per equation (5). In fact there is a doublet in the vicinity of 50MHz where the input capacitance of the EL2002 and the source resistance create the additional pole. This behavior is typical of all 0002 type buffers and whereas it is not fatal, the user should be aware of the issue.

Myth Number 2: Output Impedance

The ideal buffer should exhibit zero output impedance. Illustrated in Figure 3 is the DC output impedance of the EL2002 as a function of output current. As the load current increases, R_{OUT} asymptotically approaches the value of R1 or R2 (depending on which half of the circuit is working). In other words, the r_e term approaches zero as the emitter current increases per equation (4) above. Furthermore, Figure 4 illustrates the small signal output impedance of the EL2002 as a function of frequency. In this instance any impedances which exist at the base of Q3 (or Q4) is divided by the product of ß1*ß4, but as the frequency goes up, the ß goes down, and the R_{OUT} increases. The dip in the output impedance above 100MHz is due to capacitance of the package and on the die.

The foregoing discussion would have consequences in applications where the buffer was used “open loop” for example as a video distribution amplifier. Since R_{OUT} is both a function of output current and frequency, the gain of the circuit would vary destroying the backmatch to the coax cable thereby creating distortion.

Booby Trap Number 1: Closed Loop Operation Oscillation

Clearly, a straight forward way of avoiding the problem in the previous section is to put the buffer in a loop with an op amp or CFA as illustrated in Figure 5. Indeed, this is a classical application for a buffer when the op amp does not have enough output current to drive the desired load. What could go wrong? In some instances, depending on the bandwidth and phase margin of the amplifier and the phase shift through the buffer, the composite loop can and will oscillate. For example, the phase shift of the EL2002 is illustrated in Figure 6. At about 100MHz, it exhibits a phase lag of about 70°. When placed in a loop with an EL2044 which exhibits a nominal 60MHz bandwidth with 45° phase margin and connected for unity gain, the circuit peaks 12dB (or if you prefer **oscillates**) as shown in Figure 7. The caveat of this story is that one might expect 45° of phase lag at the -3dB bandwidth of the buffer which in the case of the EL2002 is 180MHz, but you would be wrong. Obviously, in the circuit of Figure 5, the phase margin of the EL2044 is eradicated by the phase shift of the buffer and the circuit oscillates. The moral of the story is to select an amplifier and buffer whose phase characteristics are compatible.

Another distinct possibility that can cause oscillation is the pole created by R3 and the input capacitance to A2. R3 isolates C_{IN} from the output of the op amp, but if R3 * C_{IN} is in the same order of magnitude as the unity gain crossing frequency as the op amp, you get oscillation. In this case, get the value for C_{IN} from the datasheet, and keep the value of R3 as small as possible.

Finally, given that the buffers are no more than compound emitter followers, their ability to buffer reactive loads is no better (or worse) than a conventional op amp. See Elantec Application Notes AN1092 and AN1105 for details.

Booby Trap Number 2: Closed Loop Operation

Virtually all monolithic buffers offer some sort of short circuit protection. Although not shown explicitly in Figure 5, the typical scheme senses current in R1 and R2 and limits the base drive to Q3 and Q4. Yet in some applications in spite of the manufacturer's claims of being short circuit proof, the buffer dies in the circuit. In this instance, envision a 0Ω short from the output of A2 to ground. The loop goes open and the output of A1 saturates toward the positive or negative rail. Clearly, the bases of Q3 and Q4 are “clamped” by the short to one Vbe above (or below) ground. If the base emitter breakdown voltage of Q1 or Q2 is less than the saturation voltage of A1 less a Vbe, these transistors can and will avalanche leading to self destruction.

To preclude this possibility, Elantec places a chain of back-to-back diodes (usually about 4) from input to output. This clamps the input to 4 Vbe's several volts below the rated breakdown voltage of Q1 and Q2. The moral of this story is to check with the vendor on the details of the short circuit method.

Closed Loop Buffers

Most of the pitfalls of the preceding sections can be avoided by choosing a “closed loop” buffer. One of our favorites is the EL2099 whose primary mission was intended as a video distribution amplifier. Nevertheless, it is a 50MHz Current Feedback Amplifier with output current capability of 800mA. It has all of the virtues of Figure 5 with none of the booby traps.

Conclusion

Some of the basic issues in using unity gain buffers has been presented, and armed with these details the wary and informed circuit designer can make excellent use of buffers in real and demanding applications.

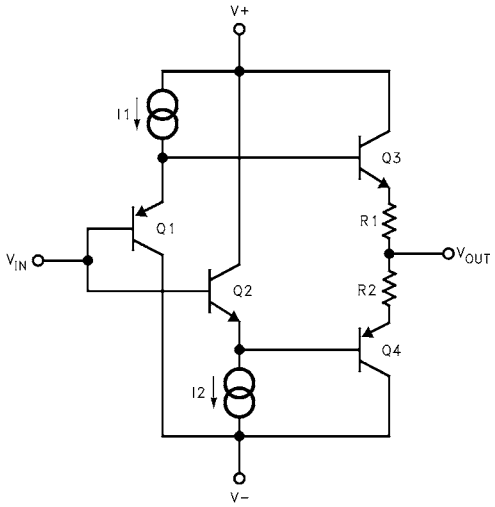

FIGURE 1. “0002” TOPOLOGY

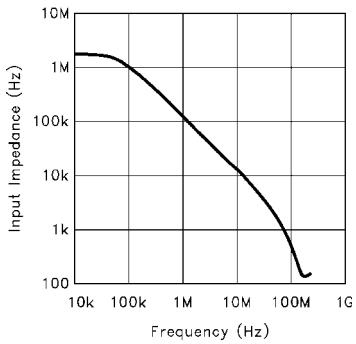

FIGURE 2. EL2002 INPUT IMPEDANCE

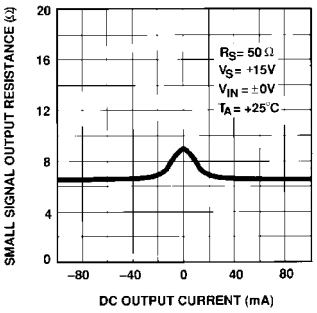

FIGURE 3. EL2002 DC OUTPUT IMPEDANCE

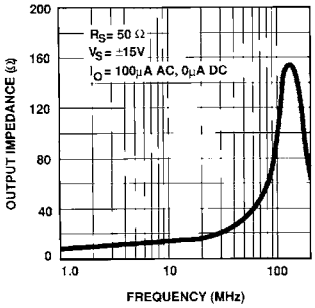

FIGURE 4. OUTPUT IMPEDANCE vs FREQUENCY

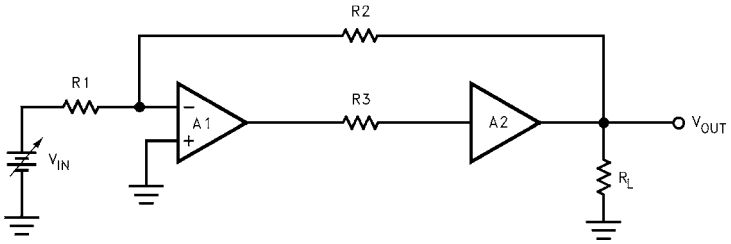

FIGURE 5. BUFFER IN A CLOSED LOOP WITH AN OP AMP

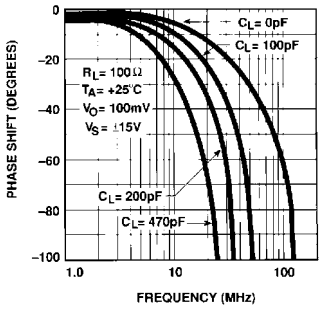

FIGURE 6. PHASE SHIFT vs FREQUENCY FOR VARIOUS CAPACITIVE LOADS

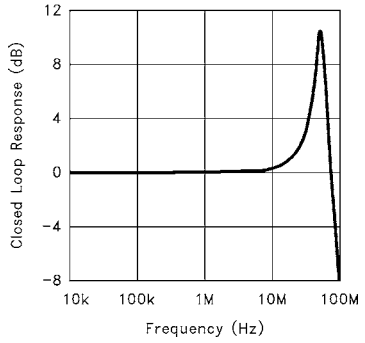

FIGURE 7. EL2044 IN LOOP WITH EL2002